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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,150	02/13/2004	Woo-jong Park	Q79322	4042

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EXAMINER	
AHMED, SALMAN	

ART UNIT	PAPER NUMBER
2419	

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01/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/777,150	**Applicant(s)** PARK, WOO-JONG	
	Examiner SALMAN AHMED	**Art Unit** 2419	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 January 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Edan Orgad/
Supervisory Patent Examiner, Art Unit 2419

Salman Ahmed
Examiner
Art Unit: 2419

Continuation of 11. does NOT place the application in condition for allowance because: 1. Applicant's arguments see pages 2-4 of the Remarks section, filed 1/7/2009, with respect to the rejections of the claims have been fully considered and are persuasive not persuasive.

2. Applicant argues (page 2) Epps fails to disclose or suggest a packet memory management unit, inter alia, for reading out a pointer of an IP packet header and a pointer of an IP packet trailer connected to the IP packet header. However, Examiner respectfully disagrees with the Applicant's assertion. Epps does indeed teach the cited limitations. Specifically, Epps teaches a packet memory management unit for reading out a pointer of an IP packet header and a pointer of an IP packet trailer connected to the IP packet header (see column 5 line 39 -47, the packet initially enters linecard control element 130 at receive FIFO 215. This FIFO buffer is employed to absorb bursts of small packets which arrive while the pipeline isn't moving fast enough to keep up. Additionally, receive FIFO 215 allows control element 130 to process packets from multiple input interfaces 111. Referring to FIG. 3, incoming packets 113 are then separated into a header portion (inherently a pointer will identify the start location/address of the header within the FIFO buffer) and a tail portion (inherently a pointer will identify the start location/address of the tail portion within the FIFO buffer) by byte counter 310, a part of receive FIFO 215. Receive FIFO 215 comprises two logically distinct FIFOs. Header portions, here simply defined as the first n bytes of the received packet, are placed in header FIFO 320. The balance of the packet, i.e., bytes n+1 through the end of the packet, are placed in tail FIFO 330). Furthermore, to further illustrate, claim 1 further teaches an apparatus for switching packets, each packet having a header portion, a corresponding tail portion, and a class of service indicator, said apparatus comprising: a pipelined switch comprising: a plurality of packet header buffers (PHBs); an equal plurality of PHB pointers, each said PHB pointer pointing to a corresponding PHB; and an equal plurality of pipeline stage circuits connected in a sequence, comprising at least a first stage circuit and a last stage circuit, wherein: each said stage circuit begins an operation substantially simultaneously with each other; each said stage circuit passes data to a next stage circuit in said sequence when every said operation performed by all said stage circuits is completed; said first stage circuit reads said header portion and stores said header portion in said corresponding PHB using said corresponding PHB pointer; and said last stage circuit outputs a modified header portion; and a receive buffer manager (RBM) comprising: a joining circuit connected to said pipelined switch wherein said modified header portion and said corresponding tail portion are joined to form a modified packet; a receive queue manager connected to said joining circuit that buffers said modified packet in a receive packet buffer and enqueues said modified packet using said class of service indicator and a plurality of receive queues; and a dequeue circuit connected to said receive queue manager and said receive packet buffer, wherein said dequeue circuit uses said class of service indicator to dequeue said modified packet to a switch fabric.

3. Applicant argues (see page 3) that Epps discloses receiving IPv4 packets, the reference fails to disclose or suggest a packet memory management unit for assembling the first data into an Internet Protocol (IP) packet. However, Examiner respectfully disagrees with the Applicant's assertion. The present claim language including the word "assembling" is broad. The claim does not specify that the packet was in some other format other then IP format prior to memory management unit processing it. As such, in view of the broadest reasonable interpretation of the claim language, Epps does indeed teach "assembling" data into IP packet. Specifically, Epps further teaches in column 5 lines 29-33, Also note that while the specific discussion herein relates to Internet Protocol version 4 (IPv4), nothing in the present invention is limited to an IPv4-only implementation. The present invention can also be practiced in connection with the forthcoming IP version 6 (IPv6); thus satisfying the limitation of packets being IP packets. Epps teaches referring to FIG. 3, after processing by network physical interface (NPI) 210, the packets are transmitted to byte counter 310 of receive FIFO 215. The exact length of the received packet is stored with the packet header by NPI 210: The header portion of the packet is, in one embodiment, the first 64 bytes (i.e., n=64) as this is enough for the pipelined switch 220 to make the appropriate switching decisions for TCP/IP and MPLS switching (column 8, lines 13-20). Epps further shows that the packet processing further down the processing step is implemented on IP packets (column 11 lines 22-30, If the packet is IP, examine the L3 header. If the L3 header is more than 20 bytes and is an IPv4 packet (i.e., it has options), the packet is forwarded to the linecard CPU. If the packet is IP, examine the results of the fetch stage checksum calculation. Decrement & check the time to live (TTL) field. Extract the destination address (for IP) or label (for MPLS switching) and the CoS and load them into the destination search register (DSR) for PLU stage 430 to search on. As such it can be seen that the "assembled" packet in FIFO buffer is indeed assembled IP packet, contrary to Applicant's assertion.

4. Claim 6 is not patentable for the same reasons cited above.

5. Applicant argues that (see pages 3 and 4) that Epps fails to disclose or suggest a packet generator for generating the IP packet from the first data. However, Examiner respectfully disagrees with the Applicant's assertion. Epps does indeed teach the cited limitations. Specifically, Epps teaches the packet memory management unit includes: a packet generator for generating the IP packet from the first data (see column 6 line 17-22 and figure 4 box 410). Epps further teaches (columns 10-11) the fetch stage (FS) 410 (FIG. 5) interfaces with receive FIFO 215, which sends the first n bytes (i.e. data), where n is a programmable value, of a packet (the header portion) to it. The FS receives the packet header and writes it (i.e. writing is interpreted as generating) into a PHB. Along with the packet header, receive FIFO 215 sends the packet length and channel number information (i.e. all interpreted as data) (in the case of linecards having multiple input interfaces 111), which are stored in packet information register 530. Receive FIFO 215 also sets a flag bit indicating if this header has a corresponding tail portion. As fetch stage 410 receives the packet header it performs the following operations. First, the FS writes the packet header into the PHB starting at the PHB offset address contained in a unique pointer assigned by the pipeline control (i.e. writing is interpreted as generating). Based on the checksum calculation, FS 410 sets (i.e. interpreted as another step implemented in the process of generating) an indication in the PCR 540 if the checksum is correct or not, which is used by PreP stage 420.

6. As such, claims 1-12 stand rejected..